

x86-TSO

## The HOL Specification

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March 25, 2009

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## **Introduction**

This document is an automatically typeset version of the HOL definition of our x86-TSO model.

## Part I

# axiomatic\_memory\_model



**type\_abbrev** Ximm : word32

**type\_abbrev** proc : num

*iiid* = { proc : proc;  
          *poi* : num }

**type\_abbrev** address : Ximm

**type\_abbrev** value : Ximm

**type\_abbrev** eiid : num

**type\_abbrev** reln : 'a#'*a* → bool

dirn = R | W

location = LOCATION\_REG **of** proc '*reg*  
          | LOCATION\_MEM **of** address

barrier = LFENCE | SFENCE | MFENCE

*action* = ACCESS **of** dirn ('*reg* location) value | BARRIER **of** barrier

event = { eiid : eiid;  
          *iiid* : *iiid*;  
          *action* : ('*reg* *action*) }

event\_structure = { *procs* : proc set;  
                  *events* : ('*reg* event)set;  
                  *intra\_causality* : ('*reg* event)reln;  
                  *atomicity* : ('*reg* event)set set }

is\_mem\_access *e* = ∃ *d a v*. *e.action* = ACCESS *d* (LOCATION\_MEM *a*) *v*

writes *E* = { *e* | *e* ∈ *E.events* ∧ ∃ *l v*. *e.action* = ACCESS W *l v* }

reads *E* = { *e* | *e* ∈ *E.events* ∧ ∃ *l v*. *e.action* = ACCESS R *l v* }

fences *E* = { *e* | *e* ∈ *E.events* ∧ (∃ *f*. *e.action* = BARRIER *f*) }

mfences  $E = \{e \mid e \in E.events \wedge (e.action = \text{BARRIER MFENCE})\}$

mem\_writes  $E = \{e \mid e \in E.events \wedge \exists a v.e.action = \text{ACCESS W (LOCATION\_MEM } a)v\}$

mem\_reads  $E = \{e \mid e \in E.events \wedge \exists a v.e.action = \text{ACCESS R (LOCATION\_MEM } a)v\}$

reg\_writes  $E = \{e \mid e \in E.events \wedge \exists p r v.e.action = \text{ACCESS W (LOCATION\_REG } p r)v\}$

reg\_reads  $E = \{e \mid e \in E.events \wedge \exists p r v.e.action = \text{ACCESS R (LOCATION\_REG } p r)v\}$

mem\_accesses  $E = \{e \mid e \in E.events \wedge (\exists d a v.e.action = \text{ACCESS } d \text{ (LOCATION\_MEM } a)v)\}$

reg\_accesses  $E = \{e \mid e \in E.events \wedge \exists d p r v.e.action = \text{ACCESS } d \text{ (LOCATION\_REG } p r)v\}$

loc  $e =$

**case**  $e.action$  **of**  
 ACCESS  $d l v \rightarrow \text{SOME } l$   
 || BARRIER  $f \rightarrow \text{NONE}$

value\_of  $e =$

**case**  $e.action$  **of**  
 ACCESS  $d l v \rightarrow \text{SOME } v$   
 || BARRIER  $f \rightarrow \text{NONE}$

proc  $e = e.iid.proc$

po\_strict  $E =$

$\{(e_1, e_2) \mid (e_1.iid.proc = e_2.iid.proc) \wedge e_1.iid.poi < e_2.iid.poi \wedge$   
 $e_1 \in E.events \wedge e_2 \in E.events\}$

po\_iico  $E = \text{po\_strict } E \cup E.intra\_causality$

well\_formed\_event\_structure  $E =$

(\* The set of events is at most countable \*)  
 countable  $E.events \wedge$

(\* there are only a finite number of processors \*)  
 (finite  $E.procs$ )  $\wedge$

(\* all events are from one of those processors \*)  
 $(\forall e \in (E.events).proc e \in E.procs) \wedge$

(\* the iid and iiid of an event (together) identify it uniquely \*)

$$(\forall e_1 e_2 \in (E.events). (e_1.eiid = e_2.eiid) \wedge (e_1.iiid = e_2.iiid) \implies (e_1 = e_2)) \wedge$$

(\* intra-instruction causality is a partial order over the events \*)  
 partial\_order ( $E.intra\_causality$ )  $E.events \wedge$

(\* ...and moreover, is \*intra\*-instruction \*)  
 $(\forall (e_1, e_2) \in (E.intra\_causality). (e_1.iiid = e_2.iiid)) \wedge$

(\* the atomicity data is a partial equivalence relation: the atomic sets of events are disjoint \*)  
 per  $E.events E.atomicity \wedge$

(\* atomic sets are \*intra\* instruction \*)  
 $(\forall es \in (E.atomicity). \forall e_1 e_2 \in es. (e_1.iiid = e_2.iiid)) \wedge$

(\* accesses to a register on a processor can only be by that processor \*)  
 $(\forall e \in (E.events). \forall p r. (loc e = \text{SOME } (\text{LOCATION\_REG } p r)) \implies (p = \text{proc } e)) \wedge$

(\* An event never comes after an infinite number of other events in program order \*)  
 finite\_prefixes (po\_iico  $E$ )  $E.events \wedge$

(\* The additional properties below hold, for the ISA fragment dealt with in [SSFN+09], and were useful for the metatheory there, but seem less essential than those above. \*)

(\* there is no intra-causality edge \*from\* a memory write \*)  
 $(\forall (e_1, e_2) \in (E.intra\_causality). e_1 \neq e_2 \implies e_1 \notin \text{mem\_writes } E) \wedge$

(\* if an instruction two events on a location and one is a write, then there must be an intra-causality edge between them. In other words, there cannot be a local race within an instruction \*)

$$\begin{aligned} & (\forall (e_1 \in \text{writes } E) e_2. \\ & \quad (e_1 \neq e_2) \wedge \\ & \quad (e_2 \in \text{writes } E \vee e_2 \in \text{reads } E) \wedge \\ & \quad (e_1.iiid = e_2.iiid) \wedge \\ & \quad (\text{loc } e_1 = \text{loc } e_2) \\ & \quad \implies \\ & \quad (e_1, e_2) \in E.intra\_causality \vee \\ & \quad (e_2, e_1) \in E.intra\_causality) \wedge \end{aligned}$$

(\* each atomic set includes all the events of its instruction \*)  
 $(\forall es \in (E.atomicity). \forall e_1 \in es. \forall e_2 \in (E.events). (e_1.iiid = e_2.iiid) \implies e_2 \in es) \wedge$

(\* all locked instructions include at least one memory read \*)  
 $(\forall es \in (E.atomicity). \exists e \in es. e \in \text{mem\_reads } E)$

execution\_witness =

$$\begin{aligned} & \llbracket \text{memory\_order} : ('reg \text{ event})\text{reln}; \\ & \quad \text{rfmap} : ('reg \text{ event})\text{reln}; \\ & \quad \text{initial\_state} : ('reg \text{ location} \rightarrow \text{value option}) \rrbracket \end{aligned}$$

previous\_writes  $E \text{ er order} =$

$$\{ew' \mid ew' \in \text{writes } E \wedge (ew', er) \in \text{order} \wedge (\text{loc } ew' = \text{loc } er)\}$$

check\_rfmap\_written  $E X =$

$$\forall(ew, er) \in (X.\text{rfmap}).$$

**if**  $ew \in \text{mem\_accesses } E$  **then**

$$ew \in \text{maximal\_elements} (\text{previous\_writes } E \text{ er } X.\text{memory\_order} \cup \\ \text{previous\_writes } E \text{ er } (\text{po\_iico } E)) \\ X.\text{memory\_order}$$

**else** (\*  $ew \in \text{reg\_accesses } E$  \*)

$$ew \in \text{maximal\_elements} (\text{previous\_writes } E \text{ er } (\text{po\_iico } E))(\text{po\_iico } E)$$

check\_rfmap\_initial  $E X =$

$$\forall er \in (\text{reads } E \setminus \text{range } X.\text{rfmap}).$$

$$(\exists l. (\text{loc } er = \text{SOME } l) \wedge (\text{value\_of } er = X.\text{initial\_state } l)) \wedge$$

$$(\text{previous\_writes } E \text{ er } X.\text{memory\_order} \cup$$

$$\text{previous\_writes } E \text{ er } (\text{po\_iico } E) = \{\})$$

reads\_from\_map\_candidates  $E \text{ rfmap} =$

$$\forall(ew, er) \in \text{rfmap}. (er \in \text{reads } E) \wedge (ew \in \text{writes } E) \wedge$$

$$(\text{loc } ew = \text{loc } er) \wedge (\text{value\_of } ew = \text{value\_of } er)$$

valid\_execution  $E X =$

$$\text{partial\_order } X.\text{memory\_order} (\text{mem\_accesses } E) \wedge$$

$$\text{linear\_order } (X.\text{memory\_order}|_{(\text{mem\_writes } E)})(\text{mem\_writes } E) \wedge$$

$$\text{finite\_prefixes } X.\text{memory\_order} (\text{mem\_accesses } E) \wedge$$

$$(\forall ew \in (\text{mem\_writes } E).$$

$$\text{finite}\{er \mid er \in E.\text{events} \wedge (\text{loc } er = \text{loc } ew) \wedge$$

$$(er, ew) \notin X.\text{memory\_order} \wedge (ew, er) \notin X.\text{memory\_order}\}) \wedge$$

$$(\forall er \in (\text{mem\_reads } E). \forall e \in (\text{mem\_accesses } E). (er, e) \in \text{po\_iico } E \implies (er, e) \in X.\text{memory\_order}) \wedge$$

$$(\forall ew_1 ew_2 \in (\text{mem\_writes } E). (ew_1, ew_2) \in \text{po\_iico } E \implies (ew_1, ew_2) \in X.\text{memory\_order}) \wedge$$

$$(\forall ew \in (\text{mem\_writes } E). \forall er \in (\text{mem\_reads } E). \forall ef \in (\text{mfences } E).$$

$$(ew, ef) \in \text{po\_iico } E \wedge (ef, er) \in \text{po\_iico } E \implies (ew, er) \in X.\text{memory\_order}) \wedge$$

$$(\forall e_1 e_2 \in (\text{mem\_accesses } E). \forall es \in (E.\text{atomicity}).$$

$$(e_1 \in es \vee e_2 \in es) \wedge (e_1, e_2) \in \text{po\_iico } E$$

$$\implies$$

$$(e_1, e_2) \in X.\text{memory\_order}) \wedge$$

$$(\forall es \in (E.\text{atomicity}). \forall e \in (\text{mem\_accesses } E \setminus es).$$

$$(\forall e' \in (es \cap \text{mem\_accesses } E). (e, e') \in X.\text{memory\_order}) \vee$$

$$(\forall e' \in (es \cap \text{mem\_accesses } E). (e', e) \in X.\text{memory\_order})) \wedge$$

$$X.\text{rfmap} \in \text{reads\_from\_map\_candidates } E \wedge$$

$$\text{check\_rfmap\_written } E X \wedge$$

$$\text{check\_rfmap\_initial } E X$$

linear\_valid\_execution  $E X =$

$$\text{linear\_order } X.\text{memory\_order} (\text{mem\_accesses } E) \wedge$$

$$\text{finite\_prefixes } X.\text{memory\_order} (\text{mem\_accesses } E) \wedge$$

$$\begin{aligned}
& (\forall er \in (\text{mem\_reads } E). \forall e \in (\text{mem\_accesses } E). (er, e) \in \text{po\_iico } E \implies (er, e) \in X.\text{memory\_order}) \wedge \\
& (\forall ew_1 ew_2 \in (\text{mem\_writes } E). (ew_1, ew_2) \in \text{po\_iico } E \implies (ew_1, ew_2) \in X.\text{memory\_order}) \wedge \\
& (\forall ew \in (\text{mem\_writes } E). \forall er \in (\text{mem\_reads } E). \forall ef \in (\text{mfences } E). \\
& \quad (ew, ef) \in \text{po\_iico } E \wedge (ef, er) \in \text{po\_iico } E \implies (ew, er) \in X.\text{memory\_order}) \wedge \\
& (\forall e_1 e_2 \in (\text{mem\_accesses } E). \forall es \in (E.\text{atomicity}). \\
& \quad (e_1 \in es \vee e_2 \in es) \wedge (e_1, e_2) \in \text{po\_iico } E \\
& \quad \implies \\
& \quad (e_1, e_2) \in X.\text{memory\_order}) \wedge \\
& (\forall es \in (E.\text{atomicity}). \forall e \in (\text{mem\_accesses } E \setminus es). \\
& \quad (\forall e' \in (es \cap \text{mem\_accesses } E). (e, e') \in X.\text{memory\_order}) \vee \\
& \quad (\forall e' \in (es \cap \text{mem\_accesses } E). (e', e) \in X.\text{memory\_order})) \wedge \\
& X.\text{rfmap} \in \text{reads\_from\_map\_candidates } E \wedge \\
& \text{check\_rfmap\_written } E X \wedge \\
& \text{check\_rfmap\_initial } E X
\end{aligned}$$

$$\begin{aligned}
\text{max\_state\_updates } E X l = & \\
& \{\text{value\_of } ew \mid ew \in \text{maximal\_elements} \\
& \quad \{ew' \mid ew' \in \text{writes } E \wedge (\text{loc } ew' = \text{SOME } l)\} \\
& \quad (\text{case } l \text{ of} \\
& \quad \quad \text{LOCATION\_MEM } a \rightarrow X.\text{memory\_order} \\
& \quad \quad \parallel \text{LOCATION\_REG } p r \rightarrow \text{po\_iico } E)\}
\end{aligned}$$

$$\begin{aligned}
& (\text{check\_final\_state } E X \text{ NONE} = \\
& \quad \neg(\text{finite } E.\text{events})) \wedge \\
& (\text{check\_final\_state } E X (\text{SOME } \text{final\_state}) = \\
& \quad \text{finite } E.\text{events} \wedge \\
& \quad (\forall l. \\
& \quad \quad \text{if } (\text{max\_state\_updates } E X l) = \{\} \text{ then} \\
& \quad \quad \quad \text{final\_state } l = X.\text{initial\_state } l \\
& \quad \quad \text{else} \\
& \quad \quad \quad \text{final\_state } l \in \text{max\_state\_updates } E X l))
\end{aligned}$$

**Part II**  
**typesetting**

$<_{order} = order$

$e <_{order} e' = (e, e') \in order$

$e \not<_{order} e' = (e, e') \notin order$

previous\_writes  $E$   $er$   $order =$   
 $\{ew' \mid ew' \in \text{writes } E \wedge ew' <_{order} er \wedge (\text{loc } ew' = \text{loc } er)\}$

check\_rfmap\_written  $E$   $X =$   
 $\forall(ew, er) \in (X.\text{rfmap}).$   
**if**  $ew \in \text{mem\_accesses } E$  **then**  
 $ew \in \text{maximal\_elements} (\text{previous\_writes } E \text{ } er (<_{X.\text{memory\_order}}) \cup$   
 $\text{previous\_writes } E \text{ } er (<_{(\text{po\_iico } E)}))$   
 $(<_{X.\text{memory\_order}})$   
**else**  $(* ew \text{ IN } \text{reg\_accesses } E *)$   
 $ew \in \text{maximal\_elements} (\text{previous\_writes } E \text{ } er (<_{(\text{po\_iico } E)})) (<_{(\text{po\_iico } E)})$

check\_rfmap\_initial  $E$   $X =$   
 $\forall er \in (\text{reads } E \setminus \text{range } X.\text{rfmap}).$   
 $(\exists l. (\text{loc } er = \text{SOME } l) \wedge (\text{value\_of } er = X.\text{initial\_state } l)) \wedge$   
 $(\text{previous\_writes } E \text{ } er (<_{X.\text{memory\_order}}) \cup$   
 $\text{previous\_writes } E \text{ } er (<_{(\text{po\_iico } E)}) = \{\})$

ve1  $E$   $X =$   
 $\text{partial\_order } (<_{X.\text{memory\_order}})(\text{mem\_accesses } E)$

ve2  $E$   $X =$   
 $\text{linear\_order } ((<_{X.\text{memory\_order}})|_{(\text{mem\_writes } E)})(\text{mem\_writes } E)$

ve3  $E$   $X =$   
 $\text{finite\_prefixes } (<_{X.\text{memory\_order}})(\text{mem\_accesses } E)$

ve4  $E$   $X =$   
 $\forall ew \in (\text{mem\_writes } E).$   
 $\text{finite}\{er \mid er \in E.\text{events} \wedge (\text{loc } er = \text{loc } ew) \wedge$   
 $er \not<_{X.\text{memory\_order}} ew \wedge ew \not<_{X.\text{memory\_order}} er\}$

ve5  $E$   $X =$   
 $\forall er \in (\text{mem\_reads } E). \forall e \in (\text{mem\_accesses } E).$   
 $er <_{(\text{po\_iico } E)} e \implies er <_{X.\text{memory\_order}} e$

ve6  $E X =$

$\forall ew_1 ew_2 \in (\text{mem\_writes } E).$

$$ew_1 <_{(\text{po.iico } E)} ew_2 \implies ew_1 <_{X.\text{memory\_order}} ew_2$$

ve7  $E X =$

$\forall ew \in (\text{mem\_writes } E). \forall er \in (\text{mem\_reads } E). \forall ef \in (\text{mfences } E).$

$$(ew <_{(\text{po.iico } E)} ef \wedge ef <_{(\text{po.iico } E)} er) \implies ew <_{X.\text{memory\_order}} er$$

ve8  $E X =$

$\forall e_1 e_2 \in (\text{mem\_accesses } E). \forall es \in (E.\text{atomicity}).$

$$((e_1 \in es \vee e_2 \in es) \wedge e_1 <_{(\text{po.iico } E)} e_2) \implies e_1 <_{X.\text{memory\_order}} e_2$$

ve9  $E X =$

$\forall es \in (E.\text{atomicity}). \forall e \in (\text{mem\_accesses } E \setminus es).$

$$(\forall e' \in (es \cap \text{mem\_accesses } E). e <_{X.\text{memory\_order}} e') \vee$$

$$(\forall e' \in (es \cap \text{mem\_accesses } E). e' <_{X.\text{memory\_order}} e)$$

ve10  $E X = \text{reads\_from\_map\_candidates } E X.\text{rfmap}$



**Part III**  
**moretypesetting**

$$f \oplus (k \mapsto v) = (k \mapsto v)f$$

**Read from memory**

$$\frac{\text{not\_blocked } s \ p \wedge (s.M \ a = \text{SOME } v) \wedge \text{no\_pending } (s.B \ p) \ a}{s \xrightarrow{\text{EVT } p \ (\text{ACCESS } R \ (\text{LOCATION\_MEM } a)v)} s}$$

**Read from write buffer**

$$\frac{\text{not\_blocked } s \ p \wedge (\exists b_1 \ b_2. (s.B \ p = b_1 \ ++[(a, v)] \ ++b_2) \wedge \text{no\_pending } b_1 \ a)}{s \xrightarrow{\text{EVT } p \ (\text{ACCESS } R \ (\text{LOCATION\_MEM } a)v)} s}$$

**Read from register**

$$\frac{(s.R \ p \ r = \text{SOME } v)}{s \xrightarrow{\text{EVT } p \ (\text{ACCESS } R \ (\text{LOCATION\_REG } p \ r)v)} s}$$

**Write to write buffer**

$$\frac{\mathbf{T}}{s \xrightarrow{\text{EVT } p \ (\text{ACCESS } W \ (\text{LOCATION\_MEM } a)v)} s \oplus \langle\langle B := s.B \oplus (p \mapsto [(a, v)] \ ++(s.B \ p)) \rangle\rangle}$$

**Write from write buffer to memory**

$$\frac{\text{not\_blocked } s \ p \wedge (s.B \ p = b \ ++[(a, v)])}{s \xrightarrow{\mathbf{TAU}} s \oplus \langle\langle M := s.M \oplus (a \mapsto \text{SOME } v); B := s.B \oplus (p \mapsto b) \rangle\rangle}$$

**Write to register**

$$\frac{\mathbf{T}}{s \xrightarrow{\text{EVT } p \ (\text{ACCESS } W \ (\text{LOCATION\_REG } p \ r)v)} s \oplus \langle\langle R := s.R \oplus (p \mapsto ((s.R \ p) \oplus (r \mapsto \text{SOME } v))) \rangle\rangle}$$

**Barrier**

$$\frac{(b = \text{MFENCE}) \implies (s.B \ p = [])}{s \xrightarrow{\text{EVT } p \ (\text{BARRIER } b)} s}$$

**Lock**

$$\frac{(s.L = \text{NONE}) \wedge (s.B \ p = [])}{s \xrightarrow{\text{LOCK } p} s \oplus \langle\langle L := \text{SOME } p \rangle\rangle}$$

**Unlock**

$$\frac{(s.L = \text{SOME } p) \wedge (s.B \ p = [])}{s \xrightarrow{\text{UNLOCK } p} s \oplus \langle\langle L := \text{NONE} \rangle\rangle}$$

## Part IV

# lts\_memory\_model

clause\_name  $x = \mathbf{T}$

machine\_state =  $\llbracket R : \text{proc} \rightarrow 'reg \rightarrow \text{value option}; (* \text{ per-processor registers } *)$   
 $M : \text{address} \rightarrow \text{value option}; (* \text{ main memory } *)$   
 $B : \text{proc} \rightarrow (\text{address}\#\text{value})\text{list}; (* \text{ per-processor write buffers } *)$   
 $L : \text{proc option}(* \text{ which processor holds the lock } *)\rrbracket$

not\_blocked  $s p = (s.L = \text{NONE}) \vee (s.L = \text{SOME } p)$

no\_pending  $b a = \neg(\exists v'. \text{MEM } (a, v') b)$

label =  $\mathbf{TAU} \mid \mathbf{EVT \ of \ proc } ('reg \ action) \mid \mathbf{LOCK \ of \ proc} \mid \mathbf{UNLOCK \ of \ proc}$

$(\forall s \ a \ v \ p.$   
 clause\_name “read-mem”  $\wedge$   
 not\_blocked  $s \ p \wedge$   
 $(s.M \ a = \text{SOME } v) \wedge$   
 no\_pending  $(s.B \ p) a$   
 $\implies$   
 machine\_trans  $s$   
 $(\text{EVT } p \ (\text{ACCESS } R \ (\text{LOCATION\_MEM } a) v))$   
 $s) \wedge$

$(\forall s \ a \ v \ p.$   
 clause\_name “read-buffer”  $\wedge$   
 not\_blocked  $s \ p \wedge$   
 $(\exists b_1 \ b_2. (s.B \ p = b_1 \ ++ [(a, v)] \ ++ b_2) \wedge \text{no\_pending } b_1 \ a)$   
 $\implies$   
 machine\_trans  $s$   
 $(\text{EVT } p \ (\text{ACCESS } R \ (\text{LOCATION\_MEM } a) v))$   
 $s) \wedge$

$(\forall s \ r \ v \ p.$   
 clause\_name “read-reg”  $\wedge$   
 $(*\text{not\_blocked } s \ p \ /\ \wedge *)$   
 $(s.R \ p \ r = \text{SOME } v)$   
 $\implies$   
 machine\_trans  $s$   
 $(\text{EVT } p \ (\text{ACCESS } R \ (\text{LOCATION\_REG } p \ r) v))$   
 $s) \wedge$

$(\forall s \ a \ v \ p \ s'.$   
 clause\_name “write-buffer”  $\wedge$   
 $(*\text{not\_blocked } s \ p \ /\ \wedge *)$   
 $(s' = \llbracket R := s.R;$   
 $M := s.M;$

$$\begin{aligned}
 & B := (p \mapsto (a, v) \in s.B \ p) s.B; \\
 & L := s.L) \\
 \implies & \\
 & \text{machine\_trans } s \\
 & \quad (\text{EVT } p \ (\text{ACCESS } W \ (\text{LOCATION\_MEM } a) v)) \\
 & \quad s') \wedge \\
 & (\forall s \ a \ v \ p \ b \ s'. \\
 & \text{clause\_name "write-mem"} \wedge \\
 & \text{not\_blocked } s \ p \wedge \\
 & (s.B \ p = b \ ++ [(a, v)]) \wedge \\
 & (s' = \langle R := s.R; \\
 & \quad M := (a \mapsto \text{SOME } v) s.M; \\
 & \quad B := (p \mapsto b) s.B; \\
 & \quad L := s.L \rangle) \\
 \implies & \\
 & \text{machine\_trans } s \ \text{TAU } s') \wedge \\
 & (\forall s \ r \ v \ p \ s'. \\
 & \text{clause\_name "write-reg"} \wedge \\
 & (*\text{not\_blocked } s \ p*) \\
 & (s' = \langle R := (p \mapsto (r \mapsto \text{SOME } v) (s.R \ p)) s.R; \\
 & \quad M := s.M; \\
 & \quad B := s.B; \\
 & \quad L := s.L \rangle) \\
 \implies & \\
 & \text{machine\_trans } s \\
 & \quad (\text{EVT } p \ (\text{ACCESS } W \ (\text{LOCATION\_REG } p \ r) v)) \\
 & \quad s') \wedge \\
 & (\forall s \ p. \\
 & \text{clause\_name "barrier"} \wedge \\
 & (*\text{not\_blocked } s \ p \ /\ \wedge *) \\
 & (s.B \ p = []) \\
 \implies & \\
 & \text{machine\_trans } s \ (\text{EVT } p \ (\text{BARRIER } \text{MFENCE})) s) \wedge \\
 & (\forall s \ p \ b. \\
 & \text{clause\_name "nop"} \wedge \\
 & (*\text{not\_blocked } s \ p \ /\ \wedge *) \\
 & b \neq \text{MFENCE} \\
 \implies & \\
 & \text{machine\_trans } s \ (\text{EVT } p \ (\text{BARRIER } b)) s) \wedge \\
 & (\forall s \ p \ s'. \\
 & \text{clause\_name "lock"} \wedge \\
 & (s.L = \text{NONE}) \wedge \\
 & (s.B \ p = []) \wedge \\
 & (s' = \langle R := s.R;
 \end{aligned}$$

$$\begin{aligned} & M := s.M; \\ & B := s.B; \\ & L := \text{SOME } p \rangle) \\ \implies & \text{machine\_trans } s \text{ (LOCK } p) s' \wedge \end{aligned}$$

$$\begin{aligned} & (\forall s \ p \ s'. \\ & \text{clause\_name "unlock" } \wedge \\ & (s.L = \text{SOME } p) \wedge \\ & (s.B \ p = []) \wedge \\ & (s' = \langle R := s.R; \\ & \quad M := s.M; \\ & \quad B := s.B; \\ & \quad L := \text{NONE} \rangle) \\ \implies & \text{machine\_trans } s \text{ (UNLOCK } p) s' \end{aligned}$$

machine\_state\_to\_state\_constraint  $s =$   
 $\lambda l.$   
**case**  $l$  **of**  
    LOCATION\_MEM  $a \rightarrow s.M \ a$   
    || LOCATION\_REG  $p \ r \rightarrow s.R \ p \ r$

machine\_final\_state  $path =$   
**if** finite  $path$  **then**  
SOME (machine\_state\_to\_state\_constraint (last  $path$ ))  
**else**  
NONE

machine\_init\_state  $sc =$   
 $\langle R := (\lambda p \ r. sc \text{ (LOCATION\_REG } p \ r));$   
     $M := (\lambda a. sc \text{ (LOCATION\_MEM } a));$   
     $B := (\lambda p. []);$   
     $L := \text{NONE} \rangle$

is\_init  $s = \exists sc. s = \text{machine\_init\_state } sc$

evt\_machine\_state =  $\langle$

- (\* Per processor registers, annotated with the event that last wrote it \*)
- $eR : \text{proc} \rightarrow 'reg \rightarrow (\text{value} \# 'reg \text{ event option}) \text{ option};$
- (\* main memory, annotated with the event that last wrote it \*)
- $eM : \text{address} \rightarrow (\text{value} \# 'reg \text{ event option}) \text{ option};$
- (\* Per processor FIFO write buffers \*)
- $eB : \text{proc} \rightarrow 'reg \text{ event list};$
- (\* Which processor holds the lock \*)
- $eL : \text{proc} \text{ option}$

⌋

evt\_not\_blocked  $s p = (s.eL = \text{NONE}) \vee (s.eL = \text{SOME } p)$

evt\_no\_pending  $b a = \neg(\exists e. \text{MEM } e b \wedge (\text{loc } e = \text{SOME } (\text{LOCATION\_MEM } a)))$

evt\_machine\_label =  
 TAU\_EVT of 'reg event  
 | REVT of 'reg event 'reg event option  
 | WEVT of 'reg event  
 | BEVT of 'reg event  
 | LOCKE of proc 'reg event set  
 | UNLOCKE of proc 'reg event set

( $\forall s a v p er ew\_opt.$   
 clause\_name "evt-read-mem"  $\wedge$   
 evt\_not\_blocked  $s p \wedge$   
 (proc  $er = p$ )  $\wedge$   
 ( $er.action = \text{ACCESS } R (\text{LOCATION\_MEM } a)v$ )  $\wedge$   
 ( $s.eM a = \text{SOME } (v, ew\_opt)$ )  $\wedge$   
 evt\_no\_pending ( $s.eB p$ )  $a$   
 $\implies$   
 evt\_machine\_trans  $s (\text{REVT } er ew\_opt)s$ )  $\wedge$

( $\forall s a v p er ew.$   
 clause\_name "evt-read-buffer"  $\wedge$   
 evt\_not\_blocked  $s p \wedge$   
 (proc  $er = p$ )  $\wedge$   
 ( $er.action = \text{ACCESS } R (\text{LOCATION\_MEM } a)v$ )  $\wedge$   
 ( $ew.action = \text{ACCESS } W (\text{LOCATION\_MEM } a)v$ )  $\wedge$   
 ( $\exists b_1 b_2. (s.eB p = b_1 ++ [ew] ++ b_2) \wedge \text{evt\_no\_pending } b_1 a$ )  
 $\implies$   
 evt\_machine\_trans  $s (\text{REVT } er (\text{SOME } ew))s$ )  $\wedge$

( $\forall s r v p er ew\_opt.$   
 clause\_name "evt-read-reg"  $\wedge$   
 (\*evt\_not\_blocked  $s p / \wedge^*$ )  
 (proc  $er = p$ )  $\wedge$   
 ( $er.action = \text{ACCESS } R (\text{LOCATION\_REG } p r)v$ )  $\wedge$   
 ( $s.eR p r = \text{SOME } (v, ew\_opt)$ )  
 $\implies$   
 evt\_machine\_trans  $s (\text{REVT } er ew\_opt)s$ )  $\wedge$

( $\forall s a v p ew s'.$   
 clause\_name "evt-write-buffer"  $\wedge$   
 (\*evt\_not\_blocked  $s p / \wedge^*$ )  
 (proc  $ew = p$ )  $\wedge$

$(ew.action = \text{ACCESS W (LOCATION\_MEM } a)v) \wedge$   
 $(s' = \langle \langle eR := s.eR;$   
 $\quad eM := s.eM;$   
 $\quad eB := (p \mapsto ew \in s.eB p)s.eB;$   
 $\quad eL := s.eL \rangle \rangle)$   
 $\implies$   
 $\text{evt\_machine\_trans } s (\text{WEVT } ew)s' \wedge$

$(\forall s a v p ew b s'.$   
 $\text{clause\_name "evt-write-mem"} \wedge$   
 $\text{evt\_not\_blocked } s p \wedge$   
 $(\text{proc } ew = p) \wedge$   
 $(ew.action = \text{ACCESS W (LOCATION\_MEM } a)v) \wedge$   
 $(s.eB p = b ++ [ew]) \wedge$   
 $(s' = \langle \langle eR := s.eR;$   
 $\quad eM := (a \mapsto \text{SOME } (v, \text{SOME } ew))s.eM;$   
 $\quad eB := (p \mapsto b)s.eB;$   
 $\quad eL := s.eL \rangle \rangle)$   
 $\implies$   
 $\text{evt\_machine\_trans } s (\text{TAUEVT } ew)s' \wedge$

$(\forall s r v p ew s'.$   
 $\text{clause\_name "evt-write-reg"} \wedge$   
 $(*\text{evt\_not\_blocked } s p /\wedge^*)$   
 $(\text{proc } ew = p) \wedge$   
 $(ew.action = \text{ACCESS W (LOCATION\_REG } p r)v) \wedge$   
 $(s' = \langle \langle eR := (p \mapsto (r \mapsto \text{SOME } (v, \text{SOME } ew))(s.eR p))s.eR;$   
 $\quad eM := s.eM;$   
 $\quad eB := s.eB;$   
 $\quad eL := s.eL \rangle \rangle)$   
 $\implies$   
 $\text{evt\_machine\_trans } s (\text{WEVT } ew)s' \wedge$

$(\forall s p eb.$   
 $\text{clause\_name "evt-barrier"} \wedge$   
 $(*\text{evt\_not\_blocked } s p /\wedge^*)$   
 $(\text{proc } eb = p) \wedge$   
 $(eb.action = \text{BARRIER MFENCE}) \wedge$   
 $(s.eB p = [])$   
 $\implies$   
 $\text{evt\_machine\_trans } s (\text{BEVT } eb)s \wedge$

$(\forall s eb.$   
 $\text{clause\_name "evt-nop"} \wedge$   
 $(*\text{not\_blocked } s p /\wedge^*)$   
 $((eb.action = \text{BARRIER SFENCE}) \vee (eb.action = \text{BARRIER LFENCE}))$   
 $\implies$   
 $\text{evt\_machine\_trans } s (\text{BEVT } eb)s \wedge$



$(\forall s p s' es.$   
 clause\_name “evt-lock”  $\wedge$   
 $(s.eL = \text{NONE}) \wedge$   
 $(s.eB p = []) \wedge$   
 $(s' = \langle eR := s.eR;$   
      $eM := s.eM;$   
      $eB := s.eB;$   
      $eL := \text{SOME } p \rangle)$   
 $\implies$   
 evt\_machine\_trans  $s$  (LOCKE  $p es$ )  $s' \wedge$

$(\forall s p s' es.$   
 clause\_name “evt-unlock”  $\wedge$   
 $(s.eL = \text{SOME } p) \wedge$   
 $(s.eB p = []) \wedge$   
 $(s' = \langle eR := s.eR;$   
      $eM := s.eM;$   
      $eB := s.eB;$   
      $eL := \text{NONE} \rangle)$   
 $\implies$   
 evt\_machine\_trans  $s$  (UNLOCKE  $p es$ )  $s'$ )

evt\_machine\_state\_to\_state\_constraint  $s =$   
 $\lambda l.$

**case**  $l$  **of**  
     LOCATION\_MEM  $a \rightarrow \text{OPTION\_MAP FST } (s.eM a)$   
     || LOCATION\_REG  $p r \rightarrow \text{OPTION\_MAP FST } (s.eR p r)$

evt\_machine\_final\_state  $path =$   
**if** finite  $path$  **then**  
 SOME (evt\_machine\_state\_to\_state\_constraint (last  $path$ ))  
**else**  
 NONE

evt\_machine\_init\_state  $sc =$   
 $\langle eR := (\lambda p r. \text{OPTION\_MAP } (\lambda v.(v, \text{NONE})) (sc (\text{LOCATION\_REG } p r)));$   
      $eM := (\lambda a. \text{OPTION\_MAP } (\lambda v.(v, \text{NONE})) (sc (\text{LOCATION\_MEM } a)));$   
      $eB := (\lambda p. []);$   
      $eL := \text{NONE} \rangle$

evt\_is\_init  $s = \exists sc. s = \text{evt\_machine\_init\_state } sc$

$(\text{get\_orig\_event } (\text{REVT } e \_) = \text{SOME } e) \wedge$   
 $(\text{get\_orig\_event } (\text{WEVT } e) = \text{SOME } e) \wedge$   
 $(\text{get\_orig\_event } (\text{BEVT } e) = \text{SOME } e) \wedge$   
 $(\text{get\_orig\_event } \_ = \text{NONE})$

$\text{locked\_segment } path\ i\ j\ p =$   
 $j + 1 \in \text{PL } path \wedge$   
 $i < j \wedge$   
 $(\exists es. \text{nth\_label } i\ path = \text{LOCKE } p\ es) \wedge$   
 $(\exists es. \text{nth\_label } j\ path = \text{UNLOCKE } p\ es) \wedge$   
 $(\forall k\ es. i < k \wedge k < j \implies \text{nth\_label } k\ path \neq \text{UNLOCKE } p\ es)$

$\text{okEpath } E\ path =$   
 $(* \text{ The REvt, WEvt and BEvt labels are exactly the set of events } *)$   
 $(E.\text{events} = \{e \mid \exists i. i + 1 \in \text{PL } path \wedge (\text{get\_orig\_event } (\text{nth\_label } i\ path) = \text{SOME } e)\}) \wedge$   
 $(* \text{ No REvt, WEvt, or BEvt appears twice as a label } *)$   
 $(\forall i\ j\ e_1\ e_2.$   
 $\quad i + 1 \in \text{PL } path \wedge j + 1 \in \text{PL } path \wedge$   
 $\quad (\text{get\_orig\_event } (\text{nth\_label } i\ path) = \text{SOME } e_1) \wedge (\text{get\_orig\_event } (\text{nth\_label } j\ path) = \text{SOME } e_2) \wedge$   
 $\quad (e_1 = e_2)$   
 $\quad \implies$   
 $\quad (i = j)) \wedge$   
 $(* \text{ The REvt, WEvt, and BEvt parts of the trace follow po\_iico } *)$   
 $(\forall (e_1, e_2) \in (\text{po\_iico } E). \exists i\ j.$   
 $\quad i < j \wedge j + 1 \in \text{PL } path \wedge$   
 $\quad (\text{get\_orig\_event } (\text{nth\_label } i\ path) = \text{SOME } e_1) \wedge (\text{get\_orig\_event } (\text{nth\_label } j\ path) = \text{SOME } e_2)) \wedge$   
 $(* \text{ atomic sets of events are properly bracketed by lock/unlock pairs } *)$   
 $(\forall es \in (E.\text{atomicity}).$   
 $\quad \exists i\ j\ p.$   
 $\quad \text{locked\_segment } path\ i\ j\ p \wedge$   
 $\quad (\{e \mid e \in es \wedge e \in \text{mem\_accesses } E\}$   
 $\quad =$   
 $\quad \{e \mid \exists k. i < k \wedge k < j \wedge$   
 $\quad \quad (\text{get\_orig\_event } (\text{nth\_label } k\ path) = \text{SOME } e) \wedge$   
 $\quad \quad e \in \text{mem\_accesses } E \wedge$   
 $\quad \quad (\text{proc } e = p)\})$ )

$\text{okMpath } path =$   
 $\text{evt\_is\_init } (\text{first } path) \wedge$   
 $\text{okpath } \text{evt\_machine\_trans } path \wedge$   
 $\forall i\ e.$   
 $i + 1 \in \text{PL } path \wedge (\text{nth\_label } i\ path = \text{WEVT } e) \wedge \text{is\_mem\_access } e$   
 $\implies$   
 $\exists j. j + 1 \in \text{PL } path \wedge i < j \wedge (\text{nth\_label } j\ path = \text{TAUEVT } e)$

$\text{erase\_state } s\ s' =$   
 $(\forall p\ r. s'.R\ p\ r = \text{OPTION\_MAP FST } (s.eR\ p\ r)) \wedge$   
 $(\forall a. s'.M\ a = \text{OPTION\_MAP FST } (s.eM\ a)) \wedge$   
 $(\forall p. (\text{LENGTH } (s'.B\ p) = \text{LENGTH } (s.eB\ p)) \wedge$   
 $\quad \forall n. n < \text{LENGTH } (s.eB\ p) \implies$   
 $\quad \exists e\ a\ v. (\text{EL } n\ (s.eB\ p) = e) \wedge$   
 $\quad \quad (\text{proc } e = p) \wedge$   
 $\quad \quad (e.\text{action} = \text{ACCESS W } (\text{LOCATION\_MEM } a)v) \wedge$

$$(s'.L = s.eL) \wedge (\text{EL } n (s'.B p) = (a, v)) \wedge$$

$$\begin{aligned} &(\text{erase\_label } (\text{TAUEVT } \_) = \text{TAU}) \wedge \\ &(\text{erase\_label } (\text{REVT } e \_) = \text{EVT } (\text{proc } e)e.action) \wedge \\ &(\text{erase\_label } (\text{WEVT } e) = \text{EVT } (\text{proc } e)e.action) \wedge \\ &(\text{erase\_label } (\text{BEVT } e) = \text{EVT } (\text{proc } e)e.action) \wedge \\ &(\text{erase\_label } (\text{LOCKE } p es) = \text{LOCK } p) \wedge \\ &(\text{erase\_label } (\text{UNLOCKE } p es) = \text{UNLOCK } p) \end{aligned}$$

$$\begin{aligned} &(\text{annotated\_labels } \text{TAU } ew e\_opt = \{\text{TAUEVT } ew\}) \wedge \\ &(\text{annotated\_labels } (\text{EVT } p (\text{ACCESS } R l v))ew e\_opt = \\ &\quad \{\text{REVT } e e\_opt \mid e \mid (e.action = \text{ACCESS } R l v) \wedge (p = \text{proc } e)\}) \wedge \\ &(\text{annotated\_labels } (\text{EVT } p (\text{ACCESS } W l v))ew e\_opt = \\ &\quad \{\text{WEVT } e \mid (e.action = \text{ACCESS } W l v) \wedge (p = \text{proc } e)\}) \wedge \\ &(\text{annotated\_labels } (\text{EVT } p (\text{BARRIER } b))ew e\_opt = \\ &\quad \{\text{BEVT } e \mid (e.action = \text{BARRIER } b) \wedge (p = \text{proc } e)\}) \wedge \\ &(\text{annotated\_labels } (\text{LOCK } p)ew e\_opt = \\ &\quad \{\text{LOCKE } p es \mid es \mid \mathbf{T}\}) \wedge \\ &(\text{annotated\_labels } (\text{UNLOCK } p)ew e\_opt = \\ &\quad \{\text{UNLOCKE } p es \mid es \mid \mathbf{T}\}) \end{aligned}$$

Part V

lts\_erasure

**Theorem 1**

$$\forall sc. \text{erase\_state } (\text{evt\_machine\_init\_state } sc)(\text{machine\_init\_state } sc)$$
**Theorem 2**

$$\begin{aligned} &\forall s \ s'. \\ &\text{erase\_state } s \ s' \\ &\implies \\ &(\text{evt\_machine\_state\_to\_state\_constraint } s = \\ &\text{machine\_state\_to\_state\_constraint } s') \end{aligned}$$
**Theorem 3**

$$\begin{aligned} &\forall l \ l' \ ew \ er\_opt. \\ &l \in \text{annotated\_labels } l' \ ew \ er\_opt \\ &\implies \\ &(l' = \text{erase\_label } l) \end{aligned}$$
**Theorem 4**

$$\begin{aligned} &\forall s_1 \ l \ s_2 \ s'_1. \\ &\text{evt\_machine\_trans } s_1 \ l \ s_2 \wedge \\ &\text{erase\_state } s_1 \ s'_1 \\ &\implies \\ &\exists s'_2. \\ &\text{erase\_state } s_2 \ s'_2 \wedge \\ &\text{machine\_trans } s'_1 \ (\text{erase\_label } l) s'_2 \end{aligned}$$
**Theorem 5**

$$\begin{aligned} &\forall s'_1 \ l' \ s'_2 \ s_1. \\ &\text{machine\_trans } s'_1 \ l' \ s'_2 \wedge \\ &\text{erase\_state } s_1 \ s'_1 \\ &\implies \\ &\exists ew \ ew\_opt. \\ &\forall l. l \in \text{annotated\_labels } l' \ ew \ ew\_opt \implies \\ &\exists s_2. \text{erase\_state } s_2 \ s'_2 \wedge \text{evt\_machine\_trans } s_1 \ l \ s_2 \end{aligned}$$

## Part VI

# linear\_valid\_execution

**Theorem 6**

$$\forall E X. \text{linear\_valid\_execution } E X \implies \text{valid\_execution } E X$$
**Theorem 7**

$$\begin{aligned} &\forall E X \text{ memory\_order}' . \\ &\text{valid\_execution } E X \wedge \\ &X.\text{memory\_order} \subseteq \text{memory\_order}' \wedge \\ &\text{linear\_order } \text{memory\_order}' (\text{mem\_accesses } E) \wedge \\ &\text{finite\_prefixes } \text{memory\_order}' (\text{mem\_accesses } E) \wedge \\ &(\forall er \in (\text{mem\_reads } E). \forall ew \in (\text{mem\_writes } E). \\ &(\text{loc } er = \text{loc } ew) \wedge (ew, er) \in \text{memory\_order}' \implies (ew, er) \in X.\text{memory\_order}) \\ &\implies \\ &\text{linear\_valid\_execution } E (X \oplus \text{memory\_order} := \text{memory\_order}') \end{aligned}$$

$$\begin{aligned} &\text{complete\_memory\_order } E \text{ memory\_order} = \\ &\text{memory\_order} \cup \\ &\{(e_1, e_2) \mid \exists ew er. (ew, er) \notin \text{memory\_order} \wedge (er, ew) \notin \text{memory\_order} \wedge \\ &\quad ew \in \text{mem\_writes } E \wedge er \in \text{mem\_reads } E \wedge (\text{loc } ew = \text{loc } er) \wedge \\ &\quad (e_1, er) \in \text{memory\_order} \wedge (ew, e_2) \in \text{memory\_order}\} \end{aligned}$$
**Theorem 8**

$$\begin{aligned} &\forall E X . \\ &\text{well\_formed\_event\_structure } E \wedge \\ &\text{valid\_execution } E X \\ &\implies \\ &\exists \text{memory\_order}' . \\ &X.\text{memory\_order} \subseteq \text{memory\_order}' \wedge \\ &\text{linear\_order } \text{memory\_order}' (\text{mem\_accesses } E) \wedge \\ &\text{finite\_prefixes } \text{memory\_order}' (\text{mem\_accesses } E) \wedge \\ &(\forall er \in (\text{mem\_reads } E). \forall ew \in (\text{mem\_writes } E). \\ &(\text{loc } er = \text{loc } ew) \wedge (ew, er) \in \text{memory\_order}' \implies (ew, er) \in X.\text{memory\_order}) \end{aligned}$$

**Part VII**

**lts\_trace**



$\text{no\_dup\_writes } path =$   
 $\forall i j ew.$   
 $\text{SUC } i \in \text{PL } path \wedge$   
 $\text{SUC } j \in \text{PL } path \wedge$   
 $(\text{nth\_label } i \text{ path} = \text{WEVT } ew) \wedge$   
 $(\text{nth\_label } j \text{ path} = \text{WEVT } ew)$   
 $\implies$   
 $(i = j)$

**Theorem 9**

$\forall path j e.$   
 $\text{okMpath } path \wedge$   
 $j + 1 \in \text{PL } path \wedge$   
 $(\text{nth\_label } j \text{ path} = \text{TAUEVT } e)$   
 $\implies$   
 $\exists i. i < j \wedge (\text{nth\_label } i \text{ path} = \text{WEVT } e) \wedge \text{is\_mem\_access } e$

**Theorem 10**

$\forall path i j ew_1 ew_2.$   
 $\text{okMpath } path \wedge$   
 $j + 1 \in \text{PL } path \wedge$   
 $i < j \wedge$   
 $(\text{proc } ew_1 = \text{proc } ew_2) \wedge$   
 $(\text{nth\_label } i \text{ path} = \text{TAUEVT } ew_1) \wedge$   
 $(\text{nth\_label } j \text{ path} = \text{TAUEVT } ew_2)$   
 $\implies$   
 $\exists k l. k < i \wedge l < j \wedge k < l \wedge$   
 $(\text{nth\_label } k \text{ path} = \text{WEVT } ew_1) \wedge (\text{nth\_label } l \text{ path} = \text{WEVT } ew_2)$

**Theorem 11**

$\forall path i e_1 e_2.$   
 $\text{okMpath } path \wedge$   
 $i + 1 \in \text{PL } path \wedge$   
 $(\text{nth\_label } i \text{ path} = \text{REVT } e_1 e_2)$   
 $\implies$   
 $\exists l v. e_1.action = \text{ACCESS } R \ l \ v$

**Theorem 12**

$\forall path i e.$   
 $\text{okMpath } path \wedge$   
 $i + 1 \in \text{PL } path \wedge$   
 $(\text{nth\_label } i \text{ path} = \text{WEVT } e)$   
 $\implies$   
 $\exists l v. e.action = \text{ACCESS } W \ l \ v$

**Theorem 13**

$\forall path i e.$   
 $\text{okMpath } path \wedge$

$$\begin{aligned}
& i + 1 \in \text{PL } path \wedge \\
& (\text{nth\_label } i \text{ path} = \text{BEVT } e) \\
& \implies \\
& \exists f. e.action = \text{BARRIER } f
\end{aligned}$$
**Theorem 14**

$$\begin{aligned}
& \forall path \ i \ e. \\
& \text{okMpath } path \wedge \\
& i + 1 \in \text{PL } path \wedge \\
& (\text{nth\_label } i \text{ path} = \text{WEVT } e) \wedge \\
& \text{is\_mem\_access } e \\
& \implies \\
& \exists j. j + 1 \in \text{PL } path \wedge i < j \wedge (\text{nth\_label } j \text{ path} = \text{TAUEVT } e)
\end{aligned}$$
**Theorem 15**

$$\begin{aligned}
& \forall path \ i \ j \ ew_1 \ ew_2. \\
& \text{okMpath } path \wedge \\
& j + 1 \in \text{PL } path \wedge \\
& i < j \wedge \\
& (\text{proc } ew_1 = \text{proc } ew_2) \wedge \\
& (\text{nth\_label } i \text{ path} = \text{WEVT } ew_1) \wedge \\
& (\text{nth\_label } j \text{ path} = \text{WEVT } ew_2) \wedge \\
& \text{is\_mem\_access } ew_1 \wedge \\
& \text{is\_mem\_access } ew_2 \wedge \\
& \text{no\_dup\_writes } path \\
& \implies \\
& \exists k \ l. l + 1 \in \text{PL } path \wedge k < l \wedge (\text{nth\_label } k \text{ path} = \text{TAUEVT } ew_1) \wedge (\text{nth\_label } l \text{ path} = \text{TAUEVT } ew_2)
\end{aligned}$$
**Theorem 16**

$$\begin{aligned}
& \forall path \ i \ j \ ef \ ew \ p \ es. \\
& \text{okMpath } path \wedge \\
& j + 1 \in \text{PL } path \wedge \\
& i < j \wedge \\
& (((\text{nth\_label } j \text{ path} = \text{BEVT } ef) \wedge (\text{proc } ef = \text{proc } ew) \wedge (ef.action = \text{BARRIER } \text{MFENCE})) \vee \\
& (\text{nth\_label } j \text{ path} = \text{UNLOCKE } (\text{proc } ew) es) \vee \\
& (\text{nth\_label } j \text{ path} = \text{LOCKE } (\text{proc } ew) es)) \wedge \\
& (\text{nth\_label } i \text{ path} = \text{WEVT } ew) \wedge \\
& \text{is\_mem\_access } ew \\
& \implies \\
& \exists k. k < j \wedge (\text{nth\_label } k \text{ path} = \text{TAUEVT } ew)
\end{aligned}$$
**Theorem 17**

$$\begin{aligned}
& \forall path \ j \ er \ ew. \\
& \text{okMpath } path \wedge \\
& j + 1 \in \text{PL } path \wedge \\
& \text{no\_dup\_writes } path \wedge \\
& (\text{nth\_label } j \text{ path} = \text{REVT } er \ (\text{SOME } ew)) \\
& \implies
\end{aligned}$$

$$\begin{aligned}
& (\text{loc } er = \text{loc } ew) \wedge \\
& (\text{value\_of } er = \text{value\_of } ew) \wedge \\
& (((\text{proc } er = \text{proc } ew) \wedge \\
& \exists i. \\
& i < j \wedge \\
& (\text{nth\_label } i \text{ path} = \text{WEVT } ew) \wedge \\
& (\forall k. i < k \wedge k < j \implies \text{nth\_label } k \text{ path} \neq \text{TAUEVT } ew) \wedge \\
& (\forall k \text{ ew}'. i < k \wedge k < j \wedge (\text{nth\_label } k \text{ path} = \text{WEVT } ew') \wedge (\text{proc } er = \text{proc } ew') \implies \\
& \quad \text{loc } ew \neq \text{loc } ew')) \vee \\
& (\exists i. \\
& i < j \wedge \\
& (\text{nth\_label } i \text{ path} = \text{TAUEVT } ew) \wedge \\
& (\forall k \text{ ew}'. k < j \wedge (\text{nth\_label } k \text{ path} = \text{WEVT } ew') \wedge (\text{proc } er = \text{proc } ew') \wedge \\
& \quad (\text{loc } ew' = \text{loc } er) \implies \\
& \quad \exists l. k < l \wedge l < j \wedge (\text{nth\_label } l \text{ path} = \text{TAUEVT } ew')) \wedge \\
& (\forall k \text{ ew}'. i < k \wedge k < j \wedge (\text{nth\_label } k \text{ path} = \text{TAUEVT } ew') \implies \text{loc } ew \neq \text{loc } ew'))))
\end{aligned}$$
**Theorem 18**

$$\begin{aligned}
& \forall \text{path } i \text{ er}. \\
& \text{okMpath } \text{path} \wedge \\
& i + 1 \in \text{PL } \text{path} \wedge \\
& (\text{nth\_label } i \text{ path} = \text{REVT } er \text{ NONE}) \\
& \implies \\
& (\text{value\_of } er = \text{evt\_machine\_state\_to\_state\_constraint } (\text{first } \text{path})(\text{the } (\text{loc } er))) \wedge \\
& \forall j \text{ ew}. \\
& j < i \wedge \\
& ((\text{nth\_label } j \text{ path} = \text{TAUEVT } ew) \vee ((\text{nth\_label } j \text{ path} = \text{WEVT } ew) \wedge (\text{proc } er = \text{proc } ew))) \\
& \implies \\
& \text{loc } ew \neq \text{loc } er
\end{aligned}$$
**Theorem 19**

$$\begin{aligned}
& \forall \text{path } i \text{ j } k \text{ p } e \text{ e}'. \\
& \text{okMpath } \text{path} \wedge \\
& \text{locked\_segment } \text{path } i \text{ k } p \wedge \\
& i < j \wedge \\
& j < k \wedge \\
& \text{is\_mem\_access } e \wedge \\
& ((\text{nth\_label } j \text{ path} = \text{REVT } e \text{ e}') \vee \\
& (\text{nth\_label } j \text{ path} = \text{TAUEVT } e)) \\
& \implies \\
& (\text{proc } e = p)
\end{aligned}$$
**Theorem 20**

$$\begin{aligned}
& \forall \text{path } i \text{ j } ew. \\
& \text{okMpath } \text{path} \wedge \\
& \text{locked\_segment } \text{path } i \text{ j } (\text{proc } ew) \wedge \\
& \text{is\_mem\_access } ew \\
& \implies \\
& ((\exists k. i < k \wedge k < j \wedge (\text{nth\_label } k \text{ path} = \text{WEVT } ew)) = \\
& (\exists k. i < k \wedge k < j \wedge (\text{nth\_label } k \text{ path} = \text{TAUEVT } ew)))
\end{aligned}$$

## Part VIII

### lts\_axiomatic\_equiv

```

(get_mem_event (TAUEVT e) = SOME e) ∧
(get_mem_event (REVT e _) =
  if is_mem_access e then
    SOME e
  else
    NONE) ∧
(get_mem_event _ = NONE)

```

```

path_to_X path =
⟦ memory_order :=
  {(e1, e2) |
    ∃j i l1 l2.
      j + 1 ∈ PL path ∧ i ≤ j ∧
      (nth_label i path = l1) ∧ (nth_label j path = l2) ∧
      (get_mem_event l1 = SOME e1) ∧ (get_mem_event l2 = SOME e2)};
  rfmap := {(ew, er) | (ew, er) | ∃i. i + 1 ∈ PL path ∧ (nth_label i path = REVT er (SOME ew))};
  initial_state := evt_machine_state_to_state_constraint (first path)⟧

```

**Theorem 21**

```

∀E path.
well_formed_event_structure E ∧
okEpath E path ∧
okMpath path
⇒
linear_valid_execution E (path_to_X path)

```

```

memL E X =
{TAUEVT e | e ∈ mem_writes E} ∪
{REVT er NONE | er ∈ mem_reads E ∧ er ∉ range X.rfmap} ∪
{REVT er (SOME ew) | er ∈ mem_reads E ∧ (ew, er) ∈ X.rfmap}

```

```

to_memL E X e =
if e ∈ mem_writes E then
  TAUEVT e
else if e ∈ mem_reads E ∧ e ∉ range X.rfmap then
  REVT e NONE
else
  REVT e (SOME (CHOICE{ew | (ew, e) ∈ X.rfmap}))

```

```

localL E X =
{REVT er NONE | er ∈ reads E ∧ er ∉ range X.rfmap} ∪
{REVT er (SOME ew) | er ∈ reads E ∧ (ew, er) ∈ X.rfmap} ∪
{WEVT e | e ∈ writes E} ∪
{BEVT e | e ∈ fences E}

```

```

to_localL E X e =

```

```

if  $e \in \text{writes } E$  then
  WEVT  $e$ 
  else if  $e \in \text{fences } E$  then
    BEVT  $e$ 
  else if  $e \in \text{reads } E \wedge e \notin \text{range } X.\text{rfmap}$  then
    REVT  $e$  NONE
  else
    REVT  $e$  (SOME (CHOICE{ $ew \mid (ew, e) \in X.\text{rfmap}$ }))

```

```

proc_es  $es = \{\text{proc } e \mid e \in es\}$ 

```

```

lockL  $E X =$ 
  {LOCKE  $p es \mid es \in E.\text{atomicity} \wedge (p \in \text{proc\_es } es)$ }  $\cup$ 
  {UNLOCKE  $p es \mid es \in E.\text{atomicity} \wedge (p \in \text{proc\_es } es)$ }

```

```

allL  $E X =$ 
  memL  $E X \cup$ 
  localL  $E X \cup$ 
  lockL  $E X$ 

```

```

(Le (TAUEVT  $e$ ) = SOME  $e$ )  $\wedge$ 
(Le (REVT  $e \_$ ) = SOME  $e$ )  $\wedge$ 
(Le (WEVT  $e$ ) = SOME  $e$ )  $\wedge$ 
(Le (BEVT  $e$ ) = SOME  $e$ )  $\wedge$ 
(Le  $\_ = \text{NONE}$ )

```

```

(Les (LOCKE  $p es$ ) = SOME  $es$ )  $\wedge$ 
(Les (UNLOCKE  $p es$ ) = SOME  $es$ )  $\wedge$ 
(Les  $\_ = \text{NONE}$ )

```

```

lo1  $E X =$ 
  {( $l, l'$ )  $\mid l \in \text{memL } E X \wedge l' \in \text{memL } E X \wedge$ 
   (the (Le  $l$ ), the (Le  $l'$ ))  $\in X.\text{memory\_order}$ }

```

```

lo1_alt  $E X =$ 
  {(to_memL  $E X e, \text{to\_memL } E X e'$ )  $\mid (e, e') \mid (e, e') \in X.\text{memory\_order}$ }

```

```

lo2  $E X =$ 
  {( $l, l'$ )  $\mid l \in \text{localL } E X \wedge l' \in \text{localL } E X \wedge$ 
   (the (Le  $l$ ), the (Le  $l'$ ))  $\in \text{po\_iico } E$ }  $\cup$ 
  {(WEVT  $e, \text{WEVT } e'$ )  $\mid \text{WEVT } e \in \text{allL } E X \wedge \text{WEVT } e' \in \text{allL } E X \wedge$ 
   ( $e, e'$ )  $\in X.\text{memory\_order} \wedge (\text{proc } e = \text{proc } e')$ }  $\cup$ 
  {( $l, \text{WEVT } e$ )  $\mid l \in \text{localL } E X \wedge \text{WEVT } e \in \text{allL } E X \wedge$ 
    $\exists e'. \text{WEVT } e' \in \text{localL } E X \wedge (\text{the } (\text{Le } l), e') \in \text{po\_iico } E \wedge$ 
   ( $e', e$ )  $\in X.\text{memory\_order} \wedge (\text{proc } e' = \text{proc } e)$ }

```

$$\begin{aligned}
\text{lo2\_alt } E X = & \\
& \{(\text{to\_localL } E X e, \text{to\_localL } E X e') \mid (e, e') \mid (e, e') \in \text{po\_iico } E\} \cup \\
& \{(\text{WEVT } e, \text{WEVT } e') \mid \text{WEVT } e \in \text{allL } E X \wedge \text{WEVT } e' \in \text{allL } E X \wedge \\
& \quad (e, e') \in X.\text{memory\_order} \wedge (\text{proc } e = \text{proc } e')\} \cup \\
& \{(\text{to\_localL } E X e'', \text{WEVT } e) \mid (e'', e) \mid \\
& \quad \text{WEVT } e \in \text{allL } E X \wedge \\
& \quad \exists e'. \text{WEVT } e' \in \text{localL } E X \wedge (e'', e') \in \text{po\_iico } E \wedge \\
& \quad (e', e) \in X.\text{memory\_order} \wedge (\text{proc } e' = \text{proc } e)\}
\end{aligned}$$

$$\begin{aligned}
\text{lo3 } E X = & \\
& \{(\text{WEVT } e, \text{TAUEVT } e) \mid \text{WEVT } e \in \text{allL } E X \wedge \text{TAUEVT } e \in \text{allL } E X\}
\end{aligned}$$

$$\begin{aligned}
\text{lo4 } E X = & \\
& \{(\text{TAUEVT } e, \text{BEVT } e') \mid \text{TAUEVT } e \in \text{allL } E X \wedge \text{BEVT } e' \in \text{allL } E X \wedge \\
& \quad e' \in \text{mfences } E \wedge (e, e') \in \text{po\_iico } E\}
\end{aligned}$$

$$\begin{aligned}
\text{lo5 } E X = & \\
& \{(\text{LOCKE } p es, \text{LOCKE } p es) \mid \text{LOCKE } p es \in \text{lockL } E X\} \cup \\
& \{(\text{UNLOCKE } p es, \text{UNLOCKE } p es) \mid \text{LOCKE } p es \in \text{lockL } E X\} \cup \\
& \{(l1, l2) \mid l1 \in \text{lockL } E X \wedge l2 \in \text{lockL } E X \wedge \\
& \quad \mathbf{the} (Les l1) \neq \mathbf{the} (Les l2) \wedge \\
& \quad \exists e_1 e_2. e_1 \in \mathbf{the} (Les l1) \wedge e_2 \in \mathbf{the} (Les l2) \wedge \\
& \quad (e_1, e_2) \in X.\text{memory\_order}\} \cup \\
& \{(\text{LOCKE } p es, \text{UNLOCKE } p es) \mid \text{LOCKE } p es \in \text{lockL } E X \wedge \text{UNLOCKE } p es \in \text{lockL } E X\}
\end{aligned}$$

$$\begin{aligned}
\text{lo6 } E X = & \\
& \{(\text{LOCKE } p es, l) \mid \text{LOCKE } p es \in \text{allL } E X \wedge l \in \text{allL } E X \wedge \\
& \quad \exists e. (\text{Le } l = \text{SOME } e) \wedge e \in es \wedge e \in \text{mem\_accesses } E\}
\end{aligned}$$

$$\begin{aligned}
\text{lo7 } E X = & \\
& \{(l, \text{UNLOCKE } p es) \mid l \in \text{memL } E X \wedge \text{UNLOCKE } p es \in \text{allL } E X \wedge \\
& \quad \exists e. (\text{Le } l = \text{SOME } e) \wedge e \in es\}
\end{aligned}$$

$$\begin{aligned}
\text{lo8 } E X = & \\
& \{(\text{UNLOCKE } p es, l) \mid \text{UNLOCKE } p es \in \text{allL } E X \wedge l \in \text{allL } E X \wedge \\
& \quad \exists e e'. (\text{Le } l = \text{SOME } e) \wedge e' \in es \wedge e \notin es \wedge \\
& \quad (e', e) \in X.\text{memory\_order} \wedge \\
& \quad (l \notin \text{memL } E X \implies ((\text{proc } e = p) \wedge e \in \text{mem\_accesses } E))\}
\end{aligned}$$

$$\begin{aligned}
\text{lo9 } E X = & \\
& \{(l, \text{LOCKE } p es) \mid l \in \text{memL } E X \wedge \text{LOCKE } p es \in \text{allL } E X \wedge \\
& \quad \exists e e'. (\text{Le } l = \text{SOME } e) \wedge e' \in es \wedge e \notin es \wedge \\
& \quad (e, e') \in X.\text{memory\_order}\}
\end{aligned}$$

$$\text{lo\_events } E X =$$

$lo1 \ E X \cup lo2 \ E X \cup$   
 $lo1 \ E X \circ lo2 \ E X \cup$   
 $lo2 \ E X \circ lo1 \ E X \cup$   
 $lo2 \ E X \circ lo1 \ E X \circ lo2 \ E X \cup$   
 $lo2 \ E X \circ lo3 \ E X \circ lo1 \ E X \cup$   
 $lo2 \ E X \circ lo3 \ E X \circ lo1 \ E X \circ lo2 \ E X \cup$   
 $lo1 \ E X \circ lo4 \ E X \circ lo2 \ E X \cup$   
 $lo2 \ E X \circ lo1 \ E X \circ lo4 \ E X \circ lo2 \ E X \cup$   
 $lo2 \ E X \circ lo3 \ E X \circ lo1 \ E X \circ lo4 \ E X \circ lo2 \ E X$

$lo68 \ E X = lo6 \ E X \cup lo8 \ E X$

$lo79 \ E X = lo7 \ E X \cup lo9 \ E X$

$lo \ E X =$   
 $lo\_events \ E X \cup$   
 $lo5 \ E X \cup$   
 $lo5 \ E X \circ lo68 \ E X \circ lo\_events \ E X \cup$   
 $lo5 \ E X \circ lo68 \ E X \circ lo\_events \ E X \cup$   
 $lo\_events \ E X \circ lo79 \ E X \circ lo5 \ E X \cup$   
 $lo\_events \ E X \circ lo79 \ E X \circ lo5 \ E X \circ lo68 \ E X \circ lo\_events \ E X$

$label\_order \ E X =$   
 $\{(l, l') \mid l \in memL \ E X \wedge l' \in memL \ E X \wedge$   
 $\quad (\mathbf{the} (Le \ l), \mathbf{the} (Le \ l')) \in X.memory\_order\} \cup$   
 $\{(l, l') \mid l \in localL \ E X \wedge l' \in localL \ E X \wedge$   
 $\quad (\mathbf{the} (Le \ l), \mathbf{the} (Le \ l')) \in po\_iico \ E\} \cup$   
 $\{(WEVT \ e, \text{TAUEVT } e) \mid WEVT \ e \in allL \ E X \wedge \text{TAUEVT } e \in allL \ E X\} \cup$   
 $\{(\text{TAUEVT } e, \text{BEVT } e') \mid \text{TAUEVT } e \in allL \ E X \wedge \text{BEVT } e' \in allL \ E X \wedge$   
 $\quad e' \in mfences \ E \wedge (e, e') \in po\_iico \ E\} \cup$   
 $\{(\text{TAUEVT } e, \text{LOCKE } p \ es) \mid \text{TAUEVT } e \in allL \ E X \wedge \text{LOCKE } p \ es \in allL \ E X \wedge$   
 $\quad e \notin es \wedge \exists e'. e' \in es \wedge e' \in mem\_accesses \ E \wedge (e, e') \in po\_iico \ E\} \cup$   
 $\{(\text{LOCKE } p \ es, l) \mid \text{LOCKE } p \ es \in allL \ E X \wedge l \in allL \ E X \wedge$   
 $\quad \exists e. (Le \ l = \text{SOME } e) \wedge e \in es \wedge e \in mem\_accesses \ E\} \cup$   
 $\{(l, \text{UNLOCKE } p \ es) \mid l \in memL \ E X \wedge \text{UNLOCKE } p \ es \in allL \ E X \wedge$   
 $\quad \exists e. (Le \ l = \text{SOME } e) \wedge e \in es\} \cup$   
 $\{(\text{UNLOCKE } p \ es, l) \mid \text{UNLOCKE } p \ es \in allL \ E X \wedge l \in allL \ E X \wedge$   
 $\quad \exists e \ e'. (Le \ l = \text{SOME } e) \wedge e' \in es \wedge e \notin es \wedge$   
 $\quad (e', e) \in X.memory\_order \wedge$   
 $\quad (l \in memL \ E X \vee (e \in mem\_accesses \ E \wedge (\text{proc } e = p)))\} \cup$   
 $\{(l, \text{LOCKE } p \ es) \mid l \in memL \ E X \wedge \text{LOCKE } p \ es \in allL \ E X \wedge$   
 $\quad \exists e \ e'. (Le \ l = \text{SOME } e) \wedge e' \in es \wedge e \notin es \wedge$   
 $\quad (e, e') \in X.memory\_order\} \cup$   
 $\{(\text{UNLOCKE } p \ es, \text{LOCKE } p' \ es') \mid \text{UNLOCKE } p \ es \in allL \ E X \wedge \text{LOCKE } p' \ es' \in allL \ E X \wedge$   
 $\quad es \neq es' \wedge \exists e \ e'. e \in es \wedge e' \in es' \wedge (e, e') \in X.memory\_order\} \cup$   
 $\{(WEVT \ e, WEVT \ e') \mid WEVT \ e \in allL \ E X \wedge WEVT \ e' \in allL \ E X \wedge$   
 $\quad (e, e') \in X.memory\_order \wedge (\text{proc } e = \text{proc } e')\}$



**Theorem 22**

$\forall E X.$   
well\_formed\_event\_structure  $E \wedge$  linear\_valid\_execution  $E X$   
 $\implies$   
partial\_order (lo  $E X$ )(allL  $E X$ )

**Theorem 23**

$\forall E X.$   
well\_formed\_event\_structure  $E \wedge$  linear\_valid\_execution  $E X$   
 $\implies$   
label\_order  $E X \subseteq$  lo  $E X$

## Part IX

# executable\_checker

**type\_abbrev** ch\_reln : ('a#'a)list

ch\_event\_structure = [ ch\_procs : proc list;  
                           ch\_events : ('reg event)list;  
                           ch\_intra\_causality : ('reg event)ch\_reln;  
                           ch\_atomicity : ('reg event)list list ]

ch\_execution\_witness = [ (\* the memory order is the transitive closure of the pairs in ch\_memory\_order \*)  
                           ch\_memory\_order : ('reg event)ch\_reln;  
                           ch\_rfmap : 'reg event → 'reg event option;  
                           ch\_initial\_state : 'reg location → value option ]

subsetL r1 r2 = ∀x y. MEM (x, y)r1 ⇒ MEM (x, y)r2

(cross[]\_ = []) ∧  
 (cross ((x, y) ∈ r)r' = MAP (λ(x', y').(x, y'))r' ++ cross r r')

tinsert (x, y)r =  
**let** left = FILTER (λ(x', y').y' = x)r **in**  
**let** right = FILTER (λ(x', y').x' = y)r **in**  
 (x, y) ∈ r ++  
 MAP (λ(x', y').(x', y))left ++  
 MAP (λ(x', y').(x, y'))right ++  
 cross left right

(tclose[]acc = acc) ∧  
 (tclose ((x, y) ∈ r)acc = tclose r (tinsert (x, y)acc))

transitiveL r =  
 ∀x y z. MEM (x, y)r ∧ MEM (y, z)r ⇒ MEM (x, z)r

cis\_mem\_access e =  
**case** e.action **of**  
   ACCESS d (LOCATION\_MEM a)v → **T**  
 || \_ → **F**

is\_mem\_write e =  
**case** e.action **of**  
   ACCESS W (LOCATION\_MEM a)v → **T**  
 || \_ → **F**

is\_mem\_read e =  
**case** e.action **of**  
   ACCESS R (LOCATION\_MEM a)v → **T**

$\parallel \_ \rightarrow \mathbf{F}$

is\_write  $e =$

**case**  $e.action$  **of**  
 ACCESS W  $l v \rightarrow \mathbf{T}$   
 $\parallel \_ \rightarrow \mathbf{F}$

is\_read  $e =$

**case**  $e.action$  **of**  
 ACCESS R  $l v \rightarrow \mathbf{T}$   
 $\parallel \_ \rightarrow \mathbf{F}$

is\_reg\_write  $e =$

**case**  $e.action$  **of**  
 ACCESS W (LOCATION\_REG  $p x$ ) $v \rightarrow \mathbf{T}$   
 $\parallel \_ \rightarrow \mathbf{F}$

is\_reg\_read  $e =$

**case**  $e.action$  **of**  
 ACCESS R (LOCATION\_REG  $p x$ ) $v \rightarrow \mathbf{T}$   
 $\parallel \_ \rightarrow \mathbf{F}$

is\_barrier  $e =$

**case**  $e.action$  **of**  
 BARRIER MFENCE  $\rightarrow \mathbf{T}$   
 $\parallel \_ \rightarrow \mathbf{F}$

check\_po\_iico *intra*  $e_1 e_2 =$

**if**  $proc\ e_1 = proc\ e_2$  **then**  
**if**  $e_1.iid.poi < e_2.iid.poi$  **then**  
 $\mathbf{T}$   
**else if**  $e_1.iid.poi = e_2.iid.poi$  **then**  
 $e_1 \neq e_2 \wedge MEM(e_1, e_2)intra$   
**else**  
 $\mathbf{F}$   
**else**  
 $\mathbf{F}$

check\_po\_iico\_in\_mo *intra mo*  $e_1 e_2 =$

**if**  $check\_po\_iico\ intra\ e_1\ e_2$  **then**  
 $MEM(e_1, e_2)mo$   
**else**  
 $\mathbf{T}$

barrier\_separated *intra barriers*  $e_1 e_2 =$

```
(proc e1 = proc e2) ∧
EXISTS (λeb. check_po_iico intra e1 eb ∧ check_po_iico intra eb e2)
  barriers
```

```
previous_writes1 er r =
MAP FST (FILTER (λ(ew, er').(er' = er) ∧ is_write ew ∧ (loc ew = loc er))r)
```

```
previous_writes2 er intra es =
FILTER (λew.(loc ew = loc er) ∧ check_po_iico intra ew er)es
```

```
check_maximal1 x xs r =
MEM x xs ∧
EVERY (λx'.if x ≠ x' then ¬(MEM (x, x')r) else T)xs
```

```
check_maximal2 x xs intra =
MEM x xs ∧
EVERY (λx'.if x ≠ x' then ¬(check_po_iico intra x x') else T)xs
```

```
check_valid_execution E X =
let mo = tclose (FILTER (λ(e1, e2).e1 ≠ e2)X.ch_memory_order)[] in
let writes = FILTER is_write E.ch_events in
let reads = FILTER is_read E.ch_events in
let mwrites = FILTER is_mem_write writes in
let mreads = FILTER is_mem_read reads in
let barriers = FILTER is_barrier E.ch_events in
let intra = tclose E.ch_intra_causality[] in
(* partial order *)
EVERY (λ(e1, e2).e1 ≠ e2)mo ∧
EVERY (λ(e1, e2).cis_mem_access e1 ∧ cis_mem_access e2 ∧
  MEM e1 E.ch_events ∧ MEM e2 E.ch_events)X.ch_memory_order ∧
(* linear order on mwrites *)
EVERY (λe1.EVERY (λe2.if e1 ≠ e2 then
  MEM (e1, e2)mo ∨ MEM (e2, e1)mo
  else
  T)
  mwrites)
  mwrites ∧
(* po_iico in memory_order *)
EVERY (λer1.EVERY (λer2. check_po_iico_in_mo intra mo er1 er2)mreads)
  mreads ∧
EVERY (λer.EVERY (λew. check_po_iico_in_mo intra mo er ew)mwrites)
  mreads ∧
EVERY (λew1.EVERY (λew2. check_po_iico_in_mo intra mo ew1 ew2)mwrites)
  mwrites ∧
EVERY (λew.
  EVERY (λer.
```

```

if barrier_separated intra barriers ew er  $\vee$ 
  EXISTS ( $\lambda es.$  MEM ew es  $\vee$  MEM er es) E.ch_atomicity then
  check_po_iico_in_mo intra mo ew er
else
  T)
  mreads)
  mwrites  $\wedge$ 
  (* atomicity *)
  EVERY ( $\lambda es.$ 
    EVERY ( $\lambda e.$ 
      if  $\neg$ (MEM e es) then
        EVERY ( $\lambda e'.$ 
          if is_mem_read e'  $\vee$  is_mem_write e' then
            MEM (e, e') mo
          else
            T)
          es  $\vee$ 
          EVERY ( $\lambda e'.$ 
            if is_mem_read e'  $\vee$  is_mem_write e' then
              MEM (e', e) mo
            else
              T)
            es
          else
            T)
        (mreads ++ mwrites))
    E.ch_atomicity  $\wedge$ 
    (* rfmc *)
    EVERY ( $\lambda er.$ 
      case X.ch_rfmap er of
        SOME ew  $\rightarrow$ 
          is_read er  $\wedge$  is_write ew  $\wedge$  MEM ew E.ch_events  $\wedge$ 
          (loc er = loc ew)  $\wedge$  (value_of er = value_of ew)
          || NONE  $\rightarrow$  T)
        E.ch_events  $\wedge$ 
        (* rfmap written and initial*)
        EVERY ( $\lambda er.$ 
          case X.ch_rfmap er of
            SOME ew  $\rightarrow$ 
              if is_mem_write ew then
                check_maximal1 ew (previous_writes1 er mo ++
                  previous_writes2 er intra writes) mo
              else
                check_maximal2 ew (previous_writes2 er intra writes) intra
            || NONE  $\rightarrow$ 
              (case loc er of
                SOME l  $\rightarrow$ 
                  (value_of er = X.ch_initial_state l)  $\wedge$ 
                  (previous_writes1 er mo = [])  $\wedge$ 

```

```

      (previous_writes2 er intra writes = [])
    || NONE → F)
  reads

```

```

check_set_eq es1 es2 = EVERY (λe. MEM e es2)es1 ∧ EVERY (λe. MEM e es1)es2

```

```

check_well_formed_event_structure E =
let intra = tclose (FILTER (λ(e1, e2).e1 ≠ e2)E.ch_intra_causality)[] in
EVERY (λe. MEM (proc e)E.ch_procs)E.ch_events ∧
EVERY (λe1.
  EVERY (λe2.
    if (e1.iid = e2.iid) ∧ (e1.eiid = e2.eiid) then
      e1 = e2
    else T)
    E.ch_events)
  E.ch_events ∧
EVERY (λ(e1, e2). MEM e1 E.ch_events ∧ MEM e2 E.ch_events)E.ch_intra_causality ∧
EVERY (λ(e1, e2).e1 ≠ e2)intra ∧
EVERY (λ(e1, e2).e1.iid = e2.iid)intra ∧
¬MEM[]E.ch_atomicity ∧
EVERY (λes. EVERY (λe. MEM e E.ch_events)es)E.ch_atomicity ∧
EVERY (λes1.
  EVERY (λes2.
    if ¬check_set_eq es1 es2 then
      EVERY (λe1. EVERY (λe2.e1 ≠ e2)es1)es2
    else
      T)
    E.ch_atomicity)
  E.ch_atomicity ∧
EVERY (λes1. EVERY (λe1. EVERY (λe2.e1.iid = e2.iid)es1)es1)E.ch_atomicity ∧
EVERY (λe.case loc e of SOME (LOCATION_REG p r) → p = proc e || _ → T)E.ch_events ∧
EVERY (λ(e1, e2).¬is_mem_write e1)intra ∧
EVERY (λe1.
  EVERY (λe2.
    if is_write e1 ∧ e1 ≠ e2 ∧ (is_write e2 ∨ is_read e2) ∧
      (e1.iid = e2.iid) ∧ (loc e1 = loc e2) then
      MEM (e1, e2)intra ∨ MEM (e2, e1)intra
    else
      T)
    E.ch_events)
  E.ch_events ∧
EVERY (λes.
  EVERY (λe1.
    EVERY (λe2.
      if e1.iid = e2.iid then MEM e2 es else T)
      E.ch_events)
    es)
  E.ch_atomicity ∧

```

EVERY ( $\lambda es. \text{EXISTS } (\lambda e. \text{is\_mem\_read } e) es$ )  $E.ch\_atomicity$

chE\_to\_E E =  
 $\langle\langle$   $procs := \text{set } E.ch\_procs;$   
 $events := \text{set } E.ch\_events;$   
 $intra\_causality :=$   
 $(\text{set } E.ch\_intra\_causality)^+ \cup \{(e, e) \mid e \in (\text{set } E.ch\_events)\};$   
 $atomicity := \text{set } (\text{MAP } \text{set } E.ch\_atomicity)\rangle\rangle$

chX\_to\_X E X =  
 $\langle\langle$   $memory\_order := (\text{set } X.ch\_memory\_order)^+ \cup$   
 $\{(e, e) \mid e \in \text{mem\_accesses } (\text{chE\_to\_E } E)\};$   
 $rfmap := \{(ew, er) \mid \text{MEM } er E.ch\_events \wedge (X.ch\_rfmap } er = \text{SOME } ew)\};$   
 $initial\_state := X.ch\_initial\_state\rangle\rangle$

**Theorem 24**

$\forall E X.$   
 $\text{well\_formed\_event\_structure } (\text{chE\_to\_E } E)$   
 $\implies$   
 $(\text{check\_valid\_execution } E X = \text{valid\_execution } (\text{chE\_to\_E } E)(\text{chX\_to\_X } E X))$

**Theorem 25**

$\forall E. \text{check\_well\_formed\_event\_structure } E = \text{well\_formed\_event\_structure } (\text{chE\_to\_E } E)$



## Part X

# correct\_typesetting

**Theorem 26**

*typesetting* \$previous\_writes =  
*axiomatic\_memory\_model* \$previous\_writes

**Theorem 27**

*typesetting* \$check\_rfmap\_written =  
*axiomatic\_memory\_model* \$check\_rfmap\_written

**Theorem 28**

*typesetting* \$check\_rfmap\_initial =  
*axiomatic\_memory\_model* \$check\_rfmap\_initial

**Theorem 29**

valid\_execution  $E X =$   
ve1  $E X \wedge$   
ve2  $E X \wedge$   
ve3  $E X \wedge$   
ve4  $E X \wedge$   
ve5  $E X \wedge$   
ve6  $E X \wedge$   
ve7  $E X \wedge$   
ve8  $E X \wedge$   
ve9  $E X \wedge$   
ve10  $E X \wedge$   
check\_rfmap\_written  $E X \wedge$   
check\_rfmap\_initial  $E X$

**Theorem 30**

$\forall s l s' x y z. \text{machine\_trans } s l s' = x / * x, z * / s \xrightarrow{l} s'$

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